UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/603,132	06/23/2000	Brian A. Vaartstra	150.00650102	3538

7590 07/30/2003

Mueting Raasch & Gerbhardt PA
PO Box 581415
Minneapolis, MN 55458

EXAMINER
LEE, EUGENE

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 07/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 20

Application Number: 09/603,132
Filing Date: June 23, 2000
Appellant(s): VAARTSTRA ET AL.

Mark J. Gebhardt
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 4/25/03.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that claims 27-44 stand or fall together.

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

5,122,923	Matsubara et al.	6-1992
6,239,460	Kuroiwa et al.	5-2001

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 27 thru 35 stand rejected under 35 U.S.C. 102(b) as being anticipated by Matsubara et al. '923. Matsubara discloses (see, for example, Fig. 1) a capacitor (semiconductor device structure) comprising a silicon substrate (substrate assembly including a surface) 1 and a

lower electrode (diffusion barrier layer) 3. In column 4, lines 24-27 and column 4, lines 24-27, Matsubara discloses the lower electrode being made from $RuSi_2$ and may consist of layers of ruthenium, ruthenium oxide, ruthenium silicide and stacked structures.

Regarding claims 32-35, Matsubara discloses (see, for example, Fig. 1 and column 3, lines 43-47) a capacitor structure comprising a lower electrode (first electrode) 3, dielectric layer (high dielectric material) 4, and upper electrode (second electrode) 5. In column 4, lines 24-27 and column 4, lines 24-27, Matsubara discloses the lower electrode being made from $RuSi_2$ and may consist of layers of ruthenium, ruthenium oxide, ruthenium silicide and stacked structures.

3. Claims 27, 28, 30 thru 33, and 36 thru 44 stand rejected under 35 U.S.C. 102(b) as being anticipated by Kuroiwa et al. '460 B1. Kuroiwa discloses (see, for example, Fig. 8 and column 13, lines 12-14) a semiconductor device structure comprising a substrate (substrate assembly) 101 and a ruthenium silicide layer (diffusion barrier layer) 132.

Regarding claims 32-33, Kuroiwa shows (see, for example, FIG. 10) a capacitor structure comprising a metal electrode (first electrode) 130, capacitor dielectric 115 and upper electrode (second electrode) 116. In column 13, lines 11-15, Kuroiwa discloses the ruthenium silicide layer 132 is formed from a portion of metal electrode 130.

Regarding claims 36 and 37, Kuroiwa discloses a semiconductor device structure (integrated circuit structure) comprising a substrate assembly including a substrate (silicon containing region) 101 and transfer gate transistors (active device) 103a, and a plug (interconnect) 111 including a ruthenium silicide layer 132.

Regarding claim 38, Kuroiwa discloses a metal electrode (conductive contact material) 130.

Regarding claims 39-44, Kuroiwa discloses an opening in the insulating film 110 that is filled by the plug 111. The aspect ratio (ratio of height to width) is clearly greater than 1.

Product-by-Process Limitations

4. While not objectionable, the Office reminds Applicant that "product by process" limitations in claims drawn to structure are directed to the product, per se, no matter how actually made. *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also, *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wethheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al.*, 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or *otherwise*. Note that applicant has the burden of proof in such cases, as the above case law makes clear. Thus, no patentable weight will be given to those process steps which do not add structural limitations to the final product.

The limitation "chemical vapor codeposited" merely recites a method of forming and does not deviate from the **structure of a diffusion barrier made of $RuSi_x$**.

(11) Response to Argument

The gist of the appellant's arguments against the anticipatory rejection is primarily based on the method used to form a diffusion barrier of $RuSi_x$ in a semiconductor device structure.

However, the method (chemical vapor codeposition) is not germane to the claims being examined in the instant application. That is, because the invention, as set forth in the claims, is clearly directed towards an apparatus. Therefore the method of making the invention does not structurally distinguish the claimed invention from the cited prior art.

On page 4, paragraph 2 of the appeal brief, the appellant argues that the diffusion barrier layer made by a method of "chemical vapor codeposition" is different than the layer made by a method of "sputtering". However, the claims, as presented in the instant application, do not state any of these structural differences. The claims only state a diffusion barrier made by a method of chemical vapor deposition and do not state at all any structural limitations that may or may not be attributed to this method. It is the claims that define a claimed invention and the appellant has not stated any of these structural limitations in the claims. On page 5, paragraph 1 of the appeal brief, the appellant has referred to a "Declaration Under 37 C.F.R. 1.132" (filed 1/27/03) that states structural differences between a sputter coating diffusion barrier layer and a chemical vapor deposited diffusion barrier layer that the appellant believe are true. However, the appellant has provided no scientific evidence to support the statements in the Declaration. The statements in the Declaration are conclusionary in nature and since the appellant has provided no factual evidence to back them up, the statements carry little weight. However, for the sake of completeness, the appellant's Declaration is assessed herein.

In paragraph 8 of the Declaration (also argued and stated on page 5, first paragraph of the appeal brief), appellant states that a sputter coated layer, with respect to high aspect ratio structures, provides different coverage thereon when compared to a chemical vapor deposited layer. Appellant further argues (see page 4, last paragraph of the appeal brief) that a chemical

vapor deposited film provides a highly conformal layer within deep contacts and other openings such as for lower electrodes of storage cell capacitors and these highly conformal layers relative to high aspect ratio structures are generally not possible with sputter coating. However, the appellant's claims do not state high aspect ratio structures or deep contacts such that a different structure from chemical vapor deposition could possibly occur. The appellant's argument that a different structure will occur because of high aspect ratio structures or deep contacts is moot here because there are no high aspect ratio structures or deep contacts limitations in the present claims. Therefore, whether the layer is laid down by chemical vapor deposition or sputtering in Matsubara's invention is irrevelant to the instant claims. In any event, a method of sputtering would also form a conformal layer on a substrate and therefore the layer would have the same structure whether laid down by sputtering or chemical vapor deposition.

On page 5, third paragraph of the appeal brief, the appellant states that sputter coated diffusion barrier layers can have a high pinhole count as compared to chemical vapor deposited diffusion barrier layers. However, it is not known what would constitute a "high" pinhole count and whether a certain amount of pinholes would definitely categorize a layer as being made by chemical vapor deposition or sputtering. The appellant has provided no factual evidence for the above assertion relating to pinholes.

On page 5, fourth paragraph of the appeal brief, the appellant states that a sputter coated diffusion barrier layer "may" have surface damage by the implantation of a metal. However, this is hypothetical and it can equally be said that the sputter coated diffusion barrier layer "may not" have surface damage. The Declaration is of little probative value on this issue. Since Matsubara discloses a simple diffusion barrier layer 3 on a flat surface, it would be reasonable to

assume that in such a simple structure, no surface damage would occur to the diffusion barrier layer. Further, Matsubara discloses (see, for example, FIG. 1) a silicon oxide layer 2 in between the substrate 1 and lower electrode 3. It is physically not possible that a metal such as ruthenium that is used to form the lower electrode 3 can implant into the substrate when there is a silicon oxide layer covering the substrate. The appellant further states in the same paragraph of the appeal brief that silicon can be implanted into platinum surfaces during sputter coating of $RuSi_x$, where the silicon can diffuse into the platinum containing substrate. However, Matsubara makes no reference to platinum in his invention.

On page 8, last paragraph of the appeal brief, the appellant states the Kuroiwa discloses many structural differences over a ruthenium silicide layer formed by silicidation. Again, the method in which the invention is made is not an issue with respect to the rejection of the claims. However, this argument will be addressed since it is related to the structural limitations regarding the diffusion barrier layer being formed of $RuSi_x$. The appellant states that chemical vapor codeposited $RuSi_x$ layer includes a more uniform distribution of silicon throughout the layer, whereas a silicidated ruthenium silicide layer exhibits a gradient of silicon content from the ruthenium/silicon interface to the opposite surface of the ruthenium layer and further a silicidated ruthenium silicide layer may include uneven island formations of silicide instead of a more uniform $RuSi_x$ formed by chemical vapor codeposition. However these statements are not supported by any evidence on the part of the appellant and are not even addressed in the Declaration. These statements are only conjecture on part of the appellant. Kuroiwa simply states a ruthenium silicide layer 132 in between a plug 111 and metal electrode 130. Kuroiwa

makes no mention of a "gradient of silicon content" or "uneven island formation of silicide" but only a uniform ruthenium silicide on top of a metal electrode 130.

On page 9, last paragraph of the appeal brief, the appellant states that claim 36 discloses an interconnect as opposed to Kuroiwa which discloses a capacitor. However, Kuroiwa clearly does show (see, FIG. 8) an interconnect comprising a plug 111, diffusion barrier 132 and electrode 130. In column 2, lines 37-41, Kuroiwa states a plug 111 being electrically connected to region 106b. Therefore, as shown in FIG. 8 and expressly disclosed by Kuroiwa, Kuroiwa clearly does show an interconnect.

On page 10, third paragraph of the appeal brief, appellant argues that Kuroiwa does not teach a diffusion barrier layer formed of $RuSi_x$, where x is in the range of about 1 to about 3. However, Kuroiwa clearly discloses a ruthenium silicide layer (as opposed to ruthenium disilicide, $RuSi_2$ or ruthenium trisilicide, $RuSi_3$) and the chemical formula for a ruthenium silicide layer is RuSi. Therefore, the ruthenium silicide of Kuroiwa clearly meets the limitation of the present claim $RuSi_x$, where x is in Kuroiwa : $RuSi_1$.

On page 11 of the appeal brief, appellant argues that Kuroiwa fails to teach that the ruthenium silicide layer 132 is on a surface defining an opening and clearly does not teach that the ruthenium silicide layer 132 is on a surface defining an opening with an aspect ratio greater than 1. However, the Examiner respectfully disagrees. In FIG. 8, Kuroiwa shows a ruthenium silicide layer 132 on a substrate (surface) 101 that defines an opening 110a. The ruthenium silicide layer defines the opening in exactly the same way as the appellant's invention (see, for example, FIGs. 5 and 6). The opening 110a clearly has an aspect ratio (ratio of height to width) greater than 1.

The method of forming a device is not germane to the issue of patentability of the device itself. The presence of process limitations on product claims can not impart patentability to the product itself.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Eugene Lee
July 14, 2003

Conferees
Eddie Lee
SPE 2815

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Olik Chaudhuri OC
SPE 2823

MUETING RAASCH & GERBHARDT PA
PO BOX 581415
MINNEAPOLIS, MN 55458